Serial No. 10/734,206 Amdt. dated <u>May 22, 2007</u> Reply to Office Action of February 22, 2007

Listing of Claims

1. (Currently Amended) An apparatus for mapping and spreading data symbols in a mobile communication system when quadrature phase shift keying modulation is performed in a mobile communication time division duplex mode, the apparatus mapping and spreading the data symbols by using binary operations, said apparatus comprising:

a binary channelized data symbol generator for generating imaginary coefficients of binary information mapped symbols;

a binary counter for counting the imaginary coefficients;

a first XOR circuit for calculating XOR values for the most significant bit and the least significant bit of the binary counter, and outputting the resulting values;

a binary scrambling code generator for mapping a scrambling code to 0 and 1, and outputting the mapped values;

a second XOR circuit for calculating XOR values for the output value from the binary scrambling code generator, the output value from the first XOR circuit, and a real coefficient of the symbol mapped by the binary channelized data symbol generator;

a mapper for mapping the values calculated by the second XOR circuit to binary numbers, and outputting the mapped values; and

a switch for outputting the output values from the mapper to a real part and an imaginary part according to the least significant bit of the binary counter, wherein the values

Docket No. P-0616

Reply to Office Action of February 22, 2007

calculated by the second XOR circuit are binary numbers such as 0 and 1 divided into a real part

and an imaginary part.

2. (Original) The apparatus of claim 1, which maps and spreads the data symbols by

using the binary operations, instead of using complex number operations, to improve efficiency

of the mobile communication system.

3. (Canceled)

4. (Original) An apparatus for mapping and spreading data symbols in a mobile

communication system, comprising:

a binary counter for counting imaginary coefficients of symbols mapped by a

binary channelized data symbol generator;

a first XOR circuit for calculating XOR values for the most significant bit and the

least significant bit of the binary counter, and outputting the resulting values;

a binary scrambling code generator for mapping a scrambling code to 0 and 1, and

outputting the mapped values;

a second XOR circuit for calculating XOR values for the output value from the

binary scrambling code generator, the output value from the first XOR circuit, and a real

coefficient of the symbol mapped by the binary channelized data symbol generator;

3

Reply to Office Action of February 22, 2007

a mapper for mapping the values calculated by the second XOR circuit to binary numbers, and outputting the mapped values; and

a switch for outputting the output values from the mapper to a real part and an imaginary part according to the least significant bit of the binary counter,

wherein the values calculated by the second XOR circuit are binary numbers divided into a real part and an imaginary part.

- 5. (Original) The apparatus of claim 4, wherein the mapper maps the binary number 0 to the binary number 1, and maps the binary number 1 to the binary number –1.
- 6. (Original) The apparatus of claim 4, wherein the binary channelized data symbol generator comprises:

a weight sign binary unit for outputting binary numbers corresponding to a sign of a weight, and outputting the binary numbers corresponding to an imaginary number of the weight;

a binary symbol unit for XORing two consecutive bit sequences, dividing the resulting values into real and imaginary parts through an inverter circuit, switching the real and imaginary parts according to the binary numbers from the weight sign binary unit corresponding to the imaginary number, and outputting the switched parts;

P. 1 CCC A .: CC

Reply to Office Action of February 22, 2007

a binary orthogonal variable spreading factor code generator for mapping an orthogonal variable spreading factor code generated by selection of a spreading factor to 0 and 1, and outputting the mapped values;

a binary channelizer for XORing the binary number from the binary symbol unit divided into the real and imaginary parts, the binary number from the weight sign binary unit and the binary number from the binary orthogonal variable spreading factor code generator, and outputting the resulting values; and

a second switch for selectively outputting the XORed values from the binary channelizer.

- 7. (Original) The apparatus of claim 6, wherein the second switch selectively outputs 0 and 1 from the binary channelizer divided into the real and imaginary parts.
- 8. (Original) The apparatus of claim 6, wherein the binary symbol unit comprises:
 a third XOR circuit for XORing the two consecutive bit sequences, and outputting the resulting values;

an inverter circuit for generating an imaginary part by inverting a bit from the third XOR circuit, and outputting the imaginary part; and

Reply to Office Action of February 22, 2007

a third switch for selectively switching an output bit from the third XOR circuit

corresponding to the real part and an output bit from the inverter circuit corresponding to the

imaginary part according to a bit for notifying the imaginary part of the weight in the weight sign

binary unit.

9. (Original) The apparatus of claim 6, wherein the binary channelizer comprises:

a fourth XOR circuit for XORing a bit for deciding the sign of the symbol

corresponding to the consecutive bit sequences in the binary symbol unit, a bit for notifying the

sign of the weight in the weight sign binary unit, and a bit sequence based on the binary

orthogonal variable spreading factor code in the binary orthogonal variable spreading factor

code generator, and outputting the resulting values;

a fifth XOR circuit for XORing a bit for notifying the imaginary number of the

weight in the weight sign binary unit and a bit sequence from the fourth XOR circuit, and

outputting the resulting values; and

a flip-flop for storing a bit corresponding to the imaginary part from the binary

symbol unit until the orthogonal variable spreading factor code is generated.

6

Amdt. dated <u>May 22, 2007</u>

Reply to Office Action of February 22, 2007

10. (Currently Amended) A method of mapping and spreading data symbols in a mobile communication system, comprising:

generating imaginary coefficients of binary information mapped symbols; counting said imaginary coefficients;

calculating first exclusive-OR values for a most significant bit and a least significant bit of the count value;

outputting said calculated first exclusive-OR values;

mapping a scrambling code to binary numbers;

outputting mapped values;

calculating second exclusive-OR values for said outputted mapped values, said outputted calculated first exclusive-OR values, and a real coefficient of one of said mapped symbols;

mapping said calculated second exclusive-OR values to binary numbers;

outputting said mapped calculated second exclusive-OR values; and

outputting said outputted mapped calculated second exclusive-OR values to at least one

of a real part or and an imaginary part according to said least significant bit; and

transmitting information from a mobile terminal based on at least one of said real part or imaginary part output according to said least significant bit.

Reply to Office Action of February 22, 2007

- 11. (Original) The method of claim 10, wherein said calculated second exclusive-OR values are binary numbers which are divided into a real part and an imaginary part.
- 12. (Original) The method of claim 10, wherein quadrature phase shift keying modulation is performed in the mobile communication system in a mobile communication time division duplex mode.
- 13. (Currently Amended) A method of mapping and spreading data symbols in a mobile communication system, comprising:

performing data symbol mapping; and

performing data symbol spreading, wherein said data symbols are mapped and spread using binary operations as follows:

generating imaginary coefficients of binary information mapped symbols;

counting said imaginary coefficients;

calculating first exclusive-OR values for a most significant bit and a least significant bit of the count value;

outputting said calculated first exclusive-OR values;

mapping a scrambling code to binary numbers;

outputting mapped values;

Reply to Office Action of February 22, 2007

calculating second exclusive-OR values for said outputted mapped values, said outputted calculated first exclusive-OR values, and a real coefficient of one of said mapped symbols;

mapping said calculated second exclusive-OR values to binary numbers;

outputting said mapped calculated second exclusive-OR values; and

outputting said outputted mapped calculated second exclusive-OR values to a real part

and an imaginary part according to said least significant bit.

14. (Canceled)

- 15. (New) A method of mapping and spreading data symbols in a mobile communication system, comprising:
- (a) generating a multiple-bit binary number based on one or more imaginary coefficients output from a data symbol generator;
- (b) logically combining predetermined bits of the multiple-bit binary number to generate a logical value;
- (c) logically combining a binary scrambling code, the logical value generated in (b), and one or more real coefficients output from the data symbol generator;
 - (d) mapping a first binary number generated in (c) to a second binary number;

- (e) selecting the second binary number to correspond to a real part or an imaginary part based on one of the predetermined bits combined in (b); and
- (f) transmitting information from a mobile terminal based on at least one of said real part or imaginary part.
- 16. (New) The method of claim 15, wherein the predetermined bits logically combined in (b) include most and least significant bits of the multiple-bit binary number generated in (a).
- 17. (New) The method of claim 15, wherein (b) is performed using an XOR logical circuit.
- 18. (New) The method of claim 15, wherein, in (d), the first binary number is one of first or second values and the second binary number is one of third or fourth values, wherein at least one of the first or second values is different from the third or fourth values.
- 19. (New) The method of claim 18, wherein the first value is 0, the second value is +1, the third value is +1, and the fourth value is -1.

Reply to Office Action of February 22, 2007

20. (New) The method of claim 15, wherein, in (e), the second binary number is selected to correspond to said real part or imaginary part based on a least significant bit of the multiple-bit binary number generated in (a).

- 21. (New) The method of claim 15, wherein the data symbol generator is a binary channelized data symbol generator.
- 22. (New) The method of claim 15, wherein the binary scrambling code logically combined in (c) is generated by:

generating a first value by logically combining an orthogonal variable spreading factor (OVSF) code, a bit corresponding to a sign of a weight value, and a bit indicative of a sign of a symbol corresponding to two bit sequences input into a binary symbol circuit;

generating a second value by logically combining a bit corresponding to an imaginary number of said weight value and the first value;

generating an imaginary part which corresponds to a logical combination of said two bit sequence; and

outputting the first value or the second value based on the imaginary part generated by the logical combination of said two bits sequences, wherein the binary scrambling code corresponds to the output first value or second value.

Reply to Office Action of February 22, 2007

- 23. (New) An apparatus for mapping and spreading data symbols in a mobile communication system, comprising:
 - a data symbol generator to generator one or more imaginary coefficients;
- a circuit to generate a multiple-bit binary number based on said one or more imaginary coefficients;
- a first logical circuit to combine predetermined bits of the multiple-bit binary number to generate a logical value;
- a second logical circuit to combine a binary scrambling code, the logical value generated by the first logical circuit, and one or more real coefficients output from the data symbol generator;
- a mapper to map a first binary number generated by the second logical circuit to a second binary number; and
- a selector to select the second binary number to correspond to a real part or an imaginary part based on one of the predetermined bits combined by the first logical circuit.
- 24. (New) The apparatus of claim 23, wherein the predetermined bits combined by the first logical circuit include most and least significant bits of the multiple-bit binary number.
- 25. (New) The apparatus of claim 23, wherein the first and second logical circuits include XOR logical circuits.

Reply to Office Action of February 22, 2007

- 26. (New) The apparatus of claim 23, wherein the first binary number is one of first or second values and the second binary number is one of third or fourth values, wherein at least one of the first or second values is different from the third or fourth values.
- 27. (New) The apparatus of claim 26, wherein the first value is 0, the second value is +1, the third value is +1, and the fourth value is -1.
- 28. (New) The apparatus of claim 23, wherein the second binary number is selected to correspond to said real part or imaginary part based on a least significant bit of the multiple-bit binary number.
- 29. (New) The apparatus of claim 23, wherein the data symbol generator is a binary channelized data symbol generator.
 - 30. (New) The apparatus of claim 23, further comprising: a binary scrambling code generator which:

generates a first value by logically combining an orthogonal variable spreading factor (OVSF) code, a bit corresponding to a sign of a weight value, and a bit indicative of a sign of a symbol corresponding to two bit sequences input into a binary symbol circuit;

Docket No. P-0616

Amdt. dated May 22, 2007

Reply to Office Action of February 22, 2007

generates a second value by logically combining a bit corresponding to an imaginary number of said weight value and the first value;

generates an imaginary part which corresponds to a logical combination of said two bit sequence; and

outputs the first value or the second value based on the imaginary part generated by the logical combination of said two bits sequences, wherein the binary scrambling code corresponds to the output first value or second value.